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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,612	03/17/2006	Lionel Guiraud	FR 030104	7659

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/572,612	GUIRAUD, LIONEL	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 9* is/are rejected.

7)☒ Claim(s) *5-8,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The abstract of the disclosure is objected to because of legal languages such as "means". Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "the," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura (WO200118962A1).

Regarding claim 1 , Fig. 4 of Kimura teaches an electronic circuit comprising differential signal input means (DP, DN, CN,CP), a combining stage

(B1-B4), a discriminating stage (B5-B8) and differential signal output means (QP, QN), wherein the discriminating stage comprises four transistors (B5-B8) each having respective first and second electrodes and a respective gate electrode for controlling a current flow between the first and second electrodes, wherein the first electrodes of the four transistors are connected to a common node (B5-B8 commonly coupled to I3), wherein the differential signal output means comprise a pair of differential output terminals (QP, QN) each connected to at least one of the second electrodes of the four transistors (QP coupled to B6 and QN couled to B7), and wherein the combining stage is arranged to convert differential input signals received by the differential signal input means into gate signals (O1N and O1P coupled to B5 and B8) respectively applied to the gate electrodes of at least some of the four transistors.

Regarding claim 2, Fig. 4 of Kimura teaches an electronic circuit as claimed in claim 1, wherein at least a first pair of gate electrodes (gates of B9 and B10 receives CN) receives a gate signal which has a common mode driven by a first differential input signal and a differential mode driven by a second differential input signal (differential signal of CP).

Regarding claim 3, Fig. 4 of Kimura teaches an electronic circuit as claimed in claim 1, wherein the gate signals applied to the respective gate electrodes of the four transistors of the discriminating stage are tri-state voltage signals (see O1P, O1N, QP, QN having three levels and maximum and

minimum levels in Fig. 3) so designed that a single one of the gate electrodes, selected from the differential input signals received by the differential signal input means, has a maximum or minimum voltage value.

Regarding claim 4, Fig. 4 of Kimura teaches an electronic circuit as claimed in claim 2 wherein a second pair of gate electrodes receives a gate signal which has a common mode driven by the second differential input signal (gates of B11 and B12 receives CP) and a differential mode driven by the first differential input signal (differential signal CN).

Regarding claim 9, Fig. 4 of Kimura teaches an electronic circuit as claimed in claim 1 for providing a latch function (B5-B8 is latch), wherein the differential signal input means (DP, DN, CN, CP) include a pair of differential input terminals (terminals for CN and CP) for receiving differential latch control signals, wherein the differential output terminals are respectively connected to the gate electrodes of two of the four transistors for applying thereto respective gate signals corresponding to differential output signals of the circuit (QP coupled to B6 gate and QN coupled to B7 gate), and wherein the combining and discriminating stages are so arranged that the gate signals provided by the combining stage have voltage levels higher than the differential output signals in a first state of the differential latch control signals (when CP is in between (2) and (4), CP is low and O1P, O1N are higher than CP) and lower than the differential

output signals in a second state of the differential latch control signals (when CP is high between (4) and (6), O1P is lower than CP).

Allowable Subject Matter

Claims 5-8 and 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Kimura teaches flip flop circuit with clock, one of ordinary skill in the art would not have been motivated to modify the teaching of Kimura to further includes, among other things, the specific of the combining stage including first and second groups of four combining transistors, first current generator means for generating a first current between a first node and a first power supply terminal, second current generator means for generating a second current between a second node and the first power supply terminal, and first, second, third and fourth resistors each having a respective first end connected to the first power supply terminal and a respective second end (claim 5), the specific of wherein each of the combining transistors has respective first and second electrodes and a respective gate electrode for controlling a current flow between the first and second electrodes, wherein the first electrodes of the four combining transistors of the first group are connected in common to the first node, and the first electrodes of the two combining transistors of the second group are connected in common to the second node (claim 10), and the specific

of combining stage comprising a first pre-combining stage, a first pre-discriminating stage, first differential signal intermediate means, a second pre-combining stage, a second pre-discriminating stage and second differential signal intermediate means (claim 11).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

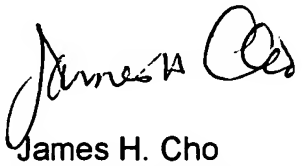
Hunt (US PAT No. 6,559,687) discloses a full rail-to-rail CMOS comparator.

Wihelm et al. (US PAT No. 4,823,030) discloses ECL logic gate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on Monday-Friday 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



James H. Cho
Primary Examiner
Art Unit 2819